Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants invention.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

Claim Objections

Applicants respectfully do not understand Examiners objection. In the previous amendment, our records show that "alignment marks" in line 4 of claim 1 was lined through and deleted.

Claim Rejections under 35 USC 102

Claims 1, 9, and 16 stand rejected under 35 USC 102(b) as being anticipated by Livengood et al. (US 5,952,247).

Livengood et al. discloses a method for **accessing a portion of a packaged integrated circuit** formed on the top of the semiconductor substrate **by etching opening through the bottom of the substrate** (see Abstract). Alignment marks are used in conjunction with a circuit diagram to determine a proper location to etch through the bottom of the **packaged chip** (see Abstract; col 3, lines 20-30). The method of Livengood et al. overcomes the problem of accessing circuitry features for probing (testing) said circuitry **following fabrication and packaging** when the top of the circuitry (bonding pads) are obscured in a packaged environment (i.e., flip chip package) (see col 2, lines 40-65; col 3, lines 13-17; col 4, lines 21-33)).

In the method of Livengood et al., Alignment marks (package fiducials) **on the package substrate** (on which chip is mounted) (item 33, Figure 3c) are used to determine the probable location of chip alignment marks on the chip (chip fiducials) (items 34, 35, Figures 3d-3e) whereby it is determined where to **etch openings through the bottom of the chip to form new alignment holes** while **fully or partially exposing** the chip alignment marks (col 6, lines 22-32).

The etching process proceeds through the bottom of chip silicon substrate to stop at a silicon-silicon dioxide interface (**silicon dioxide separating M1 from the substrate**) at the top (upper surface) of the chip (col 6, lines 33-37; col 7, lines 20-23). Livengood et al. teach **that it is not necessary to expose the entire portion of the chip alignment marks** (col 7, lines 29-34).

Livengood et al. disclose that gas assisted laser etching may be used, as well as FIB etching or laser ablation which **have the shortcoming of not accommodating endpoint detection** (col 6, lines 46-48). The chip alignment marks are then used to locate portions of the circuit on the chip and determine appropriate locations on the bottom the chip at which to etch additional openings to gain access to the circuit at the top of the chip (see e.g., col 7-col 10; claims 1, 22, 28).

Thus Livengood et al. does not disclose several elements of Applicants disclosed and claimed invention including:

"A method of re-exposing alignment marks on a **substrate through an upper surface of said substrate during semiconductor device fabrication**"

Rather, Livengood et al. discloses **fully or partially** exposing alignment marks in a **chip through a bottom of the substrate following semiconductor device fabrication.**

In addition, with respect to clams 9 and 16, Livengood et al. do not disclose a substrate upper surface comprising "at least one **transparent dielectric layer overlaying the alignment marks** and at least **one opaque layer overlaying the at least one transparent dielectric layer**", rather, Livengood et al. disclose **alignment marks** in a metal layer (M1) layer **overlying a transparent layer** (silicon dioxide) which overlies an **opaque (silicon) substrate.**

Thus, Livengood et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention;

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim Rejections under 35 USC 103

2. Claims 2, 5, 10, 13, 17 and 19 stand rejected under 35 USC 103(a) as being unpatentable over by Livengood et al., above in view of Mizumura et al. (US 5,825,035).

Applicants reiterate the comments made above with respect to Livengood et al.

The fact that Mizumura et al. disclose using an FIB system using argon ions for etching a silicon substrate without contamination does not further help Examiner in establishing a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947*

F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

3. Claims 3, 11, and 18 stand rejected under 35 USC 103(a) as being unpatentable over Livengood et al., above in view of Lee et al. (US 6,251,782).

Applicants reiterate the comments made above with respect to Livengood et al.

The fact that Lee et al. disclose a current density of 672 pA to etch silicon using an FIB system does not further help Examiner in establishing a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claims 4, 7, 8, 12 and 15 stand rejected under 35 USC 103(a) as being unpatentable over by Livengood et al., above in view of Lee et al., above, and further in view of Mizumura et al., above.

Applicants reiterate the comments made above with respect to Livengood et al., Lee et al., and Mizumura et al.

The fact that Mizumura et al. disclose using an FIB system using argon ions for etching a **silicon substrate** without contamination and Lee et al. disclose a current density of 672 pA to etch **silicon** using an FIB system does not further help Examiner in establishing a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

5. Claims 6, 14, and 20 stand rejected under 35 USC 103(a) as being unpatentable over by Livengood et al., above in view Mizumura et al., above and further in view of Lee et al., above.

Applicants reiterate the comments made above with respect to Livengood et al., Mizumura et al., and Lee et al.

The fact that Livengood et al. disclose using an FIB system to etch through the back of a silicon substrate, but teach that FIB etching has the **shortcoming of not having endpoint detection capability** and Lee discloses a current of 672 pA for FIB etching silicon does not further help Examiner in establishing a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

Based on the foregoing, Applicants respectfully request reconsideration of the Claims and submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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